

REMARKS/ARGUMENTS

Amendments were made to the specification to correct errors and to overcome objections to the drawings. No new matter has been added by any of the amendments to the specification.

Claims 1-20 are pending in the present application. Claims 1, 3, 10 and 19 were amended. Reconsideration of the claims is respectfully requested.

In a phone interview on November 14, 2006, the Examiner and Applicants' attorney discussed an Office Action in the above application that was mailed September 12, 2006. Applicants through their attorney express appreciation to the Examiner for granting this interview. Following the interview the Examiner mailed a Supplemental Office Action, on November 21, 2006. The amendments and remarks set forth herein are made in response to such Supplemental Office Action (hereinafter referred to as "Office Action").

I. Specification Amendments Made to Overcome Objections to Drawings

In the Office Action, the Examiner objected to Applicants' drawings for including reference characters that were not referred to in the specification. More particularly, Figure 1 shows a reference number 110, Figure 8 shows a reference number 800, and Figure 11 shows reference numbers 1112, 1114 and 1120, that were respectively not mentioned in the specification. Accordingly, the specification has been amended to expressly recite each of these reference numbers in association with the features to which it pertains.

II. Response to Provisional Rejection Based on Double Patenting

In the Office Action, the Examiner provisionally rejected Claims 1 and 10 on the ground of double patenting in view of co-pending U.S. Patent Application No. 10/702,994. This application and the present application are commonly assigned, and a number of inventors are common to both applications.

Enclosed herewith as Attachment A is a copy of the Filing Receipt received from the United States Patent and Trademark Office for the cited Application No. 10/702,994. The Filing Receipt shows that such application was filed on November 6, 2003, whereas the filing date of the present application was July 25, 2003. Attention is respectfully directed to **MPEP 706.02(f)(2)I**, which states in part,

"If (1) at least one common inventor exists between the applications or the applications are commonly assigned and (2) the effective filing dates are different, then a provisional rejection of the later filed application should be made." (Emphasis added).

Clearly, the present application is earlier than the cited Application No. 10/702,994, not later. Accordingly, the present application cannot be provisionally rejected in view of such Application No. 10/702,994.

III. 35 U.S.C. § 101

The Examiner has rejected claims 1-18 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. This rejection is respectfully traversed.

The Examiner asserts that Claims 1-18 may be directed to software, which is functional descriptive material, which per se is non-statutory. However, the MPEP states the following:

In this context, "functional descriptive material" consists of **data structures** and computer programs **which impart functionality when employed as a computer component**. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data.

When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Compare *In re Lowry*, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) (claim to data structure stored on a computer readable medium that increases computer efficiency held statutory) and *Warmerdam*, 33 F.3d at 1360-61, 31 USPQ2d at 1759 (claim to computer having a specific data structure stored in memory held statutory product-by-process claim) with *Warmerdam*, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure *per se* held nonstatutory). (**emphasis added**) MPEP 2106 (IV)(B)(1)

Applicants' Claim 1 recites a number of elements which unquestionably are not functional descriptive material, such as a physical port of a data processing system, and packets intended for logical ports that are received at the physical port. Even if other elements of Claim 1 pertain to functional descriptive material, Claim 1 contemplates that all such elements will be recorded on computer readable media, to enable respective recited interactions to take place with recited tangible claim elements, such as the physical port of the data processing system, and the packets to be received. Otherwise, the intended result of Claim 1 could not be realized. Thus, if any of the elements of Claim 1 are functional descriptive material, the above MPEP provision declares that such elements become "structurally and functionally interrelated to the medium and will be statutory in most cases." These conclusions apply to Claims 2-18 as well, which likewise recite key elements that are definitely not functional descriptive material.

In the above context, the term "some" means "any" computer-readable medium. The MPEP does not draw any distinctions between one type of media that is considered to be statutory and another type of

media that is considered to be non-statutory. To the contrary, the MPEP clearly states that as long as the functional descriptive material is encoded or recorded in “some” computer-readable medium, it should be considered statutory. The only exceptions to this statement in the MPEP are functional descriptive material that does not generate a useful, concrete and tangible result, e.g., functional descriptive material composed completely of pure mathematical concepts that provide no practical result. Claims 1-18 clearly recite a useful, concrete and tangible result, by emulating multiple logical ports on a physical port of a data processing system. Clearly, this result is not a disembodied mathematical concept or abstract idea. Thus, Claims 1-18 are directed to functional descriptive material that provides a useful, concrete and tangible result, and which is embodied on “some” computer-readable medium. Therefore, Claims 1-18 are statutory and the rejection thereof under 35 U.S.C. § 101 has been overcome.

Moreover, in response to Examiner’s comments regarding transmission-type media, it is noted that use of a computer readable medium such as a floppy disc or CD-ROM in a claim would clearly raise no issue of non-statutory subject matter. Devices of these types are characterized by the ability to store computer-related data for periods of time, and data can be written thereinto and be read therefrom as desired. Applicants consider that if desired, those of ordinary skill in the art could readily design and construct a computer readable medium, using currently available concepts and techniques, that had all the above characteristics of a CD-ROM or the like, and at the same time used one or more transmission-type or wireless communication links as a primary storage element. For example, the communication links could be connected to form a closed loop containing data packets in the form of electromagnetic energy. The packets would be continually circulated around the loop for a specified period of time, and data could be read therefrom and written thereinto, at will.

IV. 35 U.S.C. § 103, Obviousness

The Examiner has rejected Claims 1-5, 7, 8, and 10-16 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Publication No. 2003/0206548, to Bannai et al. (hereinafter “**Bannai**”) in view of an article entitled “*Queue Pair IP: A Hybrid Architecture for System Area Networks*,” presented by Buonadonna et al. (hereinafter “**Buonadonna**”). Claims 6 and 17 were rejected under 35 U.S.C. § 103 as being unpatentable over **Bannai**, in view of **Buonadonna** and further in view U.S. Patent Publication No. 2003/0236852 A1, to Fernandes et al. (hereinafter “**Fernandes**”). Claims 9 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over **Bannai**, in view of **Buonadonna** and an article entitled “InfiniBand”, released June 5, 2001 (hereinafter “**InfiniBand**”). Claims 19 and 20 were rejected under 35 U.S.C. § 103(a), as likewise being unpatentable over **Bannai** in view of **Buonadonna** and **InfiniBand**. These rejections are respectfully traversed.

V. Teachings of Applicants

Applicants' invention is usefully employed with a distributed computer system having the form of a system area network (SAN). The SAN includes a number of nodes that are interconnected by a switched communications fabric, which allows many devices to concurrently transfer data with high bandwidth and low latency. Host channel adapters (HCA) and target channel adapters (TCA) are located at respective nodes, and contain ports that connect to respective subnetworks or subnets of the SAN. The channel adapters further include queue pairs (QP), which are full duplex communication channels for transferring messages between channel adapter ports. In a SAN environment of the above type, there can be logical partitions (LPARs) having corresponding logical host channel adapters (LCHA). In making their invention, Applicants recognized that it would be desirable to have an efficient mechanism for associating a single physical port and queue pair with multiple logical partitions. Accordingly, Applicants provide a single, specified queue pair communication channel and its associated firmware for each physical port. Mechanisms are further provided for routing and processing all queue pair traffic pertaining to multiple logic ports by means of the single specified queue pair and physical port. Usefully, the specified queue pair is the QP zero or QP0 communication channel, as defined by InfiniBand.

The above teachings in regard to Applicants' invention are set forth in the application, such as at page 2, lines 5-13 and page 36, line 5 through page 37, line 13, and at Figure 12 of the drawings, which are as follows:

Each Queue Pair is conventionally associated with a physical port in a CA. However, it is desirable for a Host CA to be associated with multiple logical partitions of a server. Therefore, an efficient mechanism is needed to associate a single physical port and queue pair with multiple logical partitions. Therefore, it would be advantageous to have such a method, apparatus, and program to direct packets to logical partitions within a Host CA. [page 2, lines 5-13]

Multiple Logical Ports on a Single Physical Port:

The present invention operates within the SAN environment described above with regard to **Figures 1-12**. The present invention satisfies the InfiniBand requirement of a well-known QP0 communication channel being provided for each logical port on a logical HCA and also for each logical switch. Rather than including separate physical resources for each of these low-utilization communications channels, a single physical QP0 and its associated firmware are provided for each physical port. The present invention provides mechanisms for routing and processing this QP0 traffic on behalf of multiple logical ports when there is only a single QP0 associated with the physical port. An external Subnet Manager cannot distinguish the logical switches and logical HCAs with logical ports from real physical entities.

QP0 Requirements:

All logical ports/switches need to support a Subnet Management Agent (SMA) to respond to SM requests. In addition, Subnet Managers **1282-1288** may be needed to run in LPARs **1272-1278**. Also, each SM will require a QP0 to communicate with other nodes on the subnet and also logical nodes on the physical HCA. The QP that is used by a Subnet Manager running in a LPAR is referred to as an aliased QP0 **1252-1258** and is accessed using the standard IB verbs interface.

In order to support both the manager and agent in the same HCA, all received QP0 packets must first be demultiplexed to determine the intended target. These packets are received on a single QP for each physical port and are processed by hypervisor code referred to as the

Hypervisor Subnet Management Agent (HSMA) 1230. This QP is hereafter referred to as HSMA QP0. These QPs are shown as HSMA QP0 Port1 1222 and HSMA QP0 Port2 1224. Subnet Management Interface (SMI) 1260 is used to determine whether a packet is intended for a Subnet Manager or a Subnet Management Agent. [page 36, line 5 through page 37, line 13] (emphasis added)

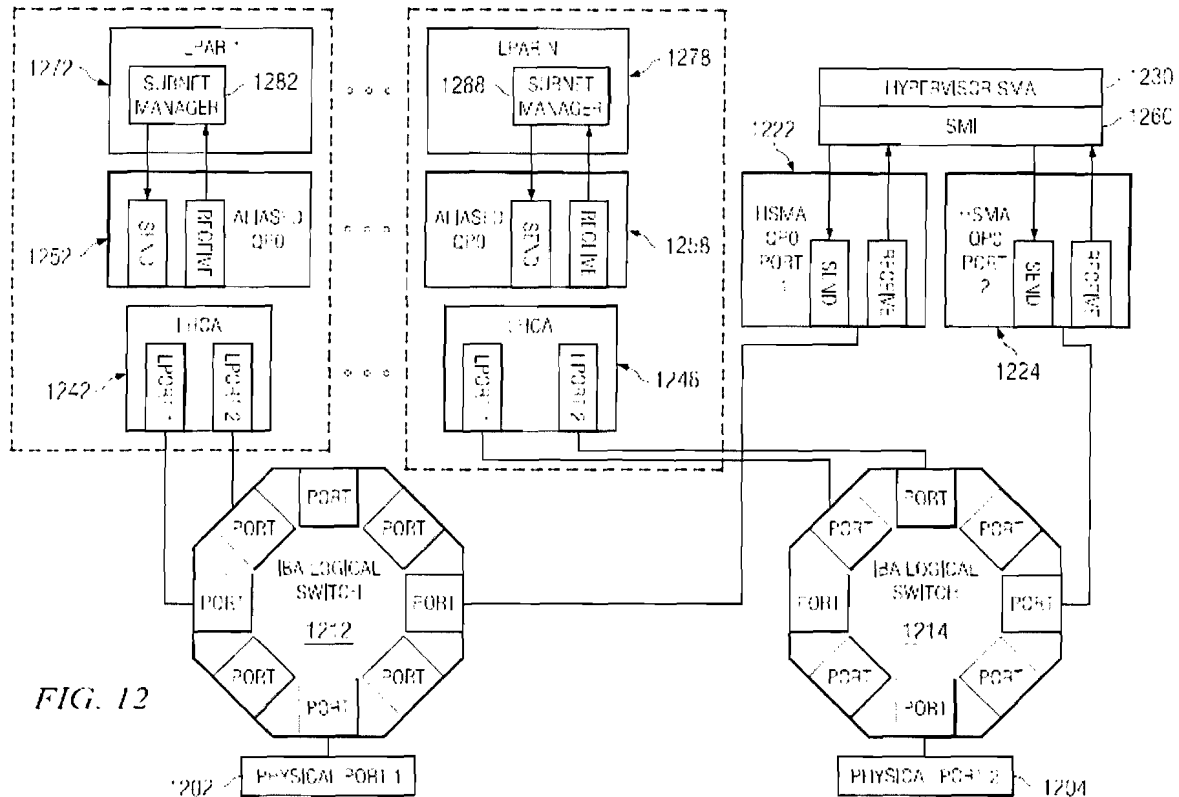


FIG. 12

One embodiment of Applicants' invention is set forth in the recitation of Claim 1, which reads as follows:

1. A method for emulating multiple logical ports on a physical port of a data processing system, the method comprising:
 - providing a subnet management queue pair for a physical port;
 - providing a plurality of logical ports, wherein packets intended for the plurality of logical ports are received at the physical port; and
 - providing an aliased subnet manager queue pair for each of the plurality of logical ports.

VI. Rejection of Claim 1

In the Office Action, the Examiner stated the following in rejecting Claim 1:

With regard to claims 1 and 10, Bannai discloses a method and apparatus for emulating multiple logical ports on a physical port (Bannai: Claim 1 provides for a method of providing multiple services over a single physical port, where the method comprises a lookup table associating a set of logical port identifiers with a set of logical ports. Therefore, multiple logical ports are associated with (or emulated on) a single physical port) comprising providing a

management interface for a physical port (Bannai: Paragraph [0035]. The management interface is associated with physical ports, and can manage the communications of the physical ports as well as the logical ports), providing a plurality of logical ports (Bannai: Claim I. As a set of logical ports is referred to in the lookup table, they are inherently provided), wherein packets intended for the plurality of logical ports are received at the physical port (Bannai: paragraph [0006]. As there is a physical port, and packets can only be initially received at a physical port, all packets that are intended for the logical ports are inherently received at the physical port), and providing an aliased subnet management interface for each of the plurality of logical ports (Bannai: paragraph [0029] and Figure 1 (314). The system port manager handles the creation and management of a logical port).

Bannai does not disclose expressly that the interface is a queue pair.

Buonadonna teaches utilizing Queue Pair IP for use in a system area network architecture (Buonadonna: Abstract).

It would have been obvious to a person of ordinary skill in the art to utilize Queue Pair IP, as taught by Buonadonna, with the logical port emulation of Bannai.

The suggestion/motivation for doing so would have been that “Queue Pair IP ... combines the interface from industry proposals for low overhead, high bandwidth networks ... with the well established inter-network protocol suite.” (Buonadonna: Abstract) Further, “with modest hardware support, QPIP can perform as well as traditional inter-network protocol implementations at a fraction of the host CPU overhead.” (Buonadonna: Abstract) **[Office Action dated 11/21/06, pages 7-8]**

Pertinent sections of **Bannai** are at paragraphs [0006], [0007], [0019], [0029] and [0035], and at Figure 1, set forth hereinafter. As particularly taught at paragraph [0019], a node 110 receives a packet from a physical port, which is apparently not shown in any drawing of **Bannai**. The node uses an identifier associated with the packet, together with a lookup table, to identify a logical port associated with the packet. The node then assigns a service to the packet based on the logical port. **Bannai** further teaches, such as at paragraphs [0029] and [0035], that a console 130 and system controller applications 302 can be operated by a user to configure a node and establish a logical port. Paragraph [0007] emphasizes that “a given logical port may include more than one physical port and span multiple physical ports”. (Emphasis added.)

[0006] In general, the present system and method alleviate port density and permit a greater number of services to be provided over a given set of physical ports by creating logical ports. Incoming data packets on a physical port may include a VLAN ID or an MPLS (Multi-Protocol Label Switching) label. The packet forwarding device assigns the incoming data packets to a specific logical port according to the VLAN ID or the MPLS label of the incoming data packet. The packet forwarding device may also assign a specific service to each logical port. Further, different customers may be assigned separate logical ports and be connected to a common physical port.

[0007] In addition, a given logical port may include more than one physical port and may span multiple physical ports on the same slot, physical ports on different slots, or physical ports on different packet forwarding devices.

[0019] In one embodiment, node 110 provides multiple services to customer A at location 120 over a single physical port of the node 110 using a logical port system and method. The node inspects incoming data packet received by the node over the single physical port and identifies a logical port identifier within data packet. Pursuant to one embodiment, the logical port identifier

[0029] The management interface 310 may comprise a graphical user interface (GUI) based interface that permits a user at the management console 130 (FIG. 1) to remotely configure, monitor, and manage the associated node. The shelf manager 312 receives data from the management interface 310, stores the information for persistency, and forwards the information to the system port manager 314. The system port manager 314 handles the creation and the management of a logical port. The system port manager 314 specifies the mode, the administrative state, the IP address, and the MAC address of the logical port and communicates with the classifier 318.

FIG. 1 is a schematic diagram of a circular system. A central circle is surrounded by four rectangular components, labeled 102, 104, 106, and 108, arranged in a square pattern. Each component is connected to a central point, labeled 120, by a line, labeled 110. The components are labeled with 'A' and 'B' in circles. A curved arrow, labeled 100, indicates a clockwise direction. A dashed line, labeled 132, is also shown.

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prima facie case, set forth in **MPEP § 2143.01**, is that the proposed modification cannot render the prior art unsatisfactory for its intended purpose.

In the present case, not all of the features of the claimed invention have been properly considered, and the teachings of the references themselves do not teach or suggest the claimed subject matter to a person of ordinary skill in the art. For example, no combination of **Bannai** and **Buonadonna** teaches or suggests, in the over-all combination of Claim 1, either of the following Claim 1 features:

- (1) Providing a subnet management queue pair for a physical port (hereinafter “Feature (1)”).
- (2) Providing an aliased subnet manager queue pair for each of the plurality of logical ports (hereinafter “Feature (2)”).

VII. Claim 1 Distinguishes Over Bannai and Buonadonna References

Features (1) and (2) of Claim 1 are clearly defined by the application, such as at **Figure 13** of Applicants’ drawings, and the specification at page 37, line 15 through page 38, line 24. Thus, **Figure 13** shows a queue pair, such as HSMA QP0 **1324**, which is associated with subnet management agent (SMA) **1330**, and is expressly provided as a communication channel for physical port **1304**. The specification teaches, at page 37, line 25 through page 38, line 5, that all traffic received from external physical port **1304** initially “is routed” to SMA **1330**, by means of subnet management queue pair **1324**. SMA **1330** then monitors such traffic, and decodes respective packets to determine their final destinations. Thus, Applicants’ specification defines the subnet management queue pair of Feature (1) to be a queue pair communication channel, for transferring packets between its associated physical port and its associated subnet management agent, which decodes the packets.

In regard to Feature (2) of Claim 1, **Figure 13** shows an aliased subnet manager queue pair, identified as aliased QP0 **1352**, provided for a plurality of logical ports LPORT1 and LPORT2. Queue pair **1352** is shown to be an aliased QP communication channel extending between the logical ports LPORT1 and LPORT2 and subnet manager **1382**, the subnet manager provided for logical partition **1372**. At page 38, lines 5-13, Applicants’ specification teaches that if a packet decoded by subnet management agent **1330** is to be routed to subnet manager **1382** of logical partition **1372**, it must be transmitted thereto, from one of the logical ports, by means of aliased queue pair 1352. Accordingly, the aliased subnet manager queue pair, recited by Feature (2) of Claim 1, is defined by the specification to be a queue pair communication channel for transmitting traffic between its associated logical ports and its associated subnet manager. Moreover, it is readily apparent that in order to achieve the Claim 1 purpose of emulating multiple logical ports on a physical port, the combined effects of both Feature (1) and Feature (2) are absolutely essential.

Bannai, of course, provides no disclosure and makes no reference whatsoever to queue pairs, nor to logical partitions, distributed computer systems or channel adapters, all of which pertain to Applicants' claims and the environment in which Applicants' invention is practiced. Applicants consider that in view of these deficiencies, those of skill in the art would readily be directed away from using the **Bannai** disclosure in an effort to realize Applicants' Claim 1.

Even without considering the above limitations of Applicants' claims, however, **Bannai** still discloses an arrangement that has little or no resemblance to the combination of features and elements recited by Claim 1. For example, in reciting the subnet management queue pair of Feature (1), Claim 1 requires a first communication channel for a physical port, wherein the first communication channel is associated with a subnet management agent. In reciting the aliased subnet manager queue pair of Feature (2), Claim 1 similarly requires a second communication channel for a plurality of logical ports, wherein the second communication channel is associated with a subnet manager. In contrast to these requirements of Claim 1, **Bannai** discloses a single node such as node 108 or 110, that receives a packet over a physical port. Nothing further is said about the physical port, or about any means for receiving the packet from the physical port. After receiving the packet, the node identifies a logical port identifier within the packet, and takes any further required action. At paragraphs [0026] and [0027], **Bannai** teaches that elements shown by Figures 2 and 3 are respectively included in a node, such as node 108. Thus, the clear teaching and emphasis of **Bannai** is the use of a single node component, to perform a series of tasks with respect to a packet. Such teaching in no way discloses or suggests the Claim 1 requirement of first and second communication channels, associated with two different managing entities.

The **Buonadonna** reference clearly does not overcome the deficiencies of **Bannai**, as discussed above in regard to Claim 1. **Buonadonna**, in fact, is principally concerned with departing from the InfiniBand architecture, which provides a hardware message passing mechanism, as discussed on page 1, lines 14-23 of the application, and is the architecture associated with queue pairs such as those of Applicants' claims. Instead, **Buonadonna**, as taught in its abstract, seeks to develop a hybrid architecture called QPIP, and to implement "basic queue pair operations over a subset of TCP, UDP and IPv6 protocols." In the paragraph bridging pages 2 and 3 of the **Buonadonna** reference, **Buonadonna** states, referring to the strategy of InfiniBand, that the "QP architecture seeks to invert this strategy and make inter-network protocols the core transport underneath the QP model." Moreover, **Buonadonna** nowhere shows or suggests a subnet management queue pair for a physical port, as recited by Feature (1) of Claim 1. Neither does **Buonadonna** show or suggest an aliased subnet manager queue pair for each of a plurality of logical ports, as recited by Feature (2).

It is noted that the Office Action did not explain how particular elements of **Buonadonna** could be combined with **Bannai** to realize either Feature (1) or Feature (2) of Applicants' Claim 1, nor did it provide any indication as to what the particular elements would be.

Since neither the **Bannai** nor the **Buonadonna** reference shows or suggests Feature (1) or Feature (2) of Claim 1, it is readily apparent that no combination of such references can show or suggest either of these features. Moreover, Applicants consider that neither the InfiniBand nor the **Fernandes** reference referred to above, in any combination with one another or with **Bannai** or **Buonadonna**, can overcome the deficiencies discussed above in regard to **Bannai** and **Buonadonna**.

VIII. No Basis Provided for Combining References to Reject Claim 1

In order to reject Claim 1 for obviousness under 35 U.S.C. § 103, by combining **Bannai** and **Buonadonna** as proposed by the Examiner, the Examiner must first demonstrate that there is some basis or motivation in the prior art for making the combination. Applicants consider that the Examiner has not done this in the Office Action. However, courts continue to hold that it is absolutely essential to provide such prior art motivation, in order to establish a *prima facie* case of obviousness by combining references. For example, in an opinion of the U.S. Court of Appeals for the Federal Circuit (CAFC), decided in January, 2005, the Court stated the following:

"Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *Dembiczak*, 175 F.3d at 999; see also *Ruiz*, 234 F.3d at 665 (explaining that the temptation to engage in impermissible hindsight is especially strong with seemingly simple mechanical inventions). This is because "combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight." [*286] *Dembiczak*, 175 F.3d at 999. Therefore, we have consistently held that a person [**9] of ordinary skill in the art must not only have had some motivation to combine the prior art teachings, but some motivation to combine the prior art teachings in the particular manner claimed. See, e.g., *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000) ("Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." (emphasis added)); *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998) ("In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." (emphasis added)). *Teleflex, Inc. v. KSR Int'l Co.*, 119 Fed. Appx. 282, 285-286 (Fed. Cir. 2005).

In the Office Action, no basis was provided for combining **Bannai** with **Buonadonna** to reject Claim 1, except for a reference to the **Buonadonna** abstract. However, the **Buonadonna** abstract in no way discloses or suggests combining teachings thereof with an arrangement such as **Bannai** in order to achieve the Applicants' Claim 1. To the contrary, the **Buonadonna** abstract expressly teaches that it

would be desirable to replace the InfiniBand architecture and the queue pairs thereof with a different hybrid architecture using QPIP. Thus, a central purpose of **Buonadonna** is to move away from the architectural environment in which the invention defined by Applicants' claims is to be practiced. In view of this, it is seen that the abstract, as well as other portions of **Buonadonna**, clearly teach away from any combination with **Bannai** to provide Applicants' Claim 1.

The *Teleflex v. KSR* opinion emphasizes that "the requirement for a showing of the teaching or motivation to combine prior art references" is particularly important when considering inventions that appear to be simple. The opinion states that for simple inventions, "the temptation to engage in impermissible hindsight is especially strong." Applicants consider that the recitation of their Claim 1, because it is comparatively brief, may be considered "simple." Accordingly, in view of the above opinion of the CAFC, Claim 1 cannot be rejected by combining **Bannai** and **Buonadonna** without a "rigorous application" of the requirement to teach a motivation for such combination.

IX. Claim 10 and 19 Distinguish Over Cited References

Independent Claim 10 recites features similar to those of Claim 1, and is considered to patentably distinguish over the cited references for the same reasons given in support thereof.

Moreover, as stated above in connection with paragraph [0007] of **Bannai**, an essential objective of **Bannai** is to enable a given logical port to include or associate with more than one physical port. However, an important purpose of Applicants' invention is to associate multiple logical partitions and their logical ports with a single physical port of a queue pair. This is taught in the specification, such as at page 2, lines 8-10 and page 36, lines 8-41, and at **Figure 12**. To emphasize this purpose, Claim 10 has been amended to recite apparatus for emulating multiple logical ports on a single physical port, wherein packets intended for each of the plurality of logical ports are received only at the single physical port. Clearly, amended Claim 10 distinguishes over any combination of references that include **Bannai**, if such combination would require modification of **Bannai** to correspond with Claim 10. Such modification would prevent **Bannai** from achieving the objective set forth in its paragraph [0007], and thus limit its capabilities in a manner not intended by **Bannai**.

Amended Claim 19 is considered to recite features similar to the patentable features of amended Claim 10, and thus distinguishes over the art for the same reasons given in support thereof. In addition, Claim 19 is considered to further distinguish over the art in reciting each queue pair thereof to be a queue pair zero. None of the cited references discloses queue pair zero communication channels. The InfiniBand reference teaches that InfiniBand specifies a serial (bit-at-a-time) bus, that the serial bus can carry multiple channels of data at the same time in the multiplexing signal, and that InfiniBand

transmissions begin or end with a channel adapter. However, such reference provides no teaching in regard to the queue pair zero recitation of Claim 19.

X. Remaining Claims Distinguish Over Cited Art

Claims 2-9 and 11-18 depend from Claims 1 and 10, respectively, and are each considered to patentably distinguish over the art for the same reasons given in support thereof.

In addition, Claim 3 is considered to distinguish over the art in reciting the sending of a packet from an aliased subnet manager queue pair, wherein the aliased queue pair comprises a queue pair zero. As stated above, the cited references including the InfiniBand reference fails to disclose use of a queue pair comprising a queue pair zero.

Claims 6 and 19 are considered to additionally distinguish over the art in reciting that each aliased subnet manager queue pair is associated with a logical partition. Applicants consider that no combination of the cited references discloses or suggests this feature.

Claims 9 and 18 are additionally considered to distinguish over the art in reciting that each sub-management queue pair is an InfiniBand queue pair zero. Applicants consider that no combination of the cited references discloses or suggests this feature.

Claim 20 depends from independent Claim 19, and is considered to patentably distinguish over the art for reasons given in support thereof.

XI. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: December 12, 2006

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/702,994	11/06/2003	2661	1184	AUS920030635US1	12	43	3

CONFIRMATION NO. 9688

35525

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Date Mailed: 02/06/2004

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Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 02/06/2004

Projected Publication Date: 05/12/2005

Non-Publication Request: No

Early Publication Request: No

Title

Infiniband general services queue pair virtualization for multiple logical ports on a single physical port

Preliminary Class

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